

**MOTOROLA SEMICONDUCTOR TECHNICAL DATA**

**BU207  
BU208**

**Designers Data Sheet**

**HORIZONTAL DEFLECTION TRANSISTOR**

... specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage –  
V<sub>CEX</sub> = 1300 Vdc – BU207  
1500 Vdc – BU208
- Collector-Emitter Sustaining Voltage –  
V<sub>CEO(sus)</sub> = 600 Vdc – BU207  
700 Vdc – BU208
- Switching Times with Inductive Loads, t<sub>f</sub> = 0.4 μs (Typ) @  
I<sub>C</sub> = 4.5 A
- Optimum Drive Condition Curves
- Glass Base-Collector Junction

**5 AMPERE  
NPN SILICON  
POWER TRANSISTORS  
1300 AND 1500 VOLTS**

**Designer's Data for  
"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

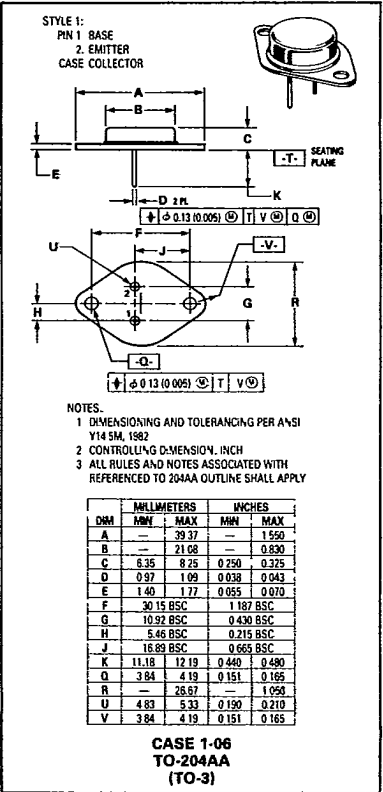
**\*MAXIMUM RATINGS**

Rating	Symbol	BU207	BU208	Unit
Collector-Emitter Voltage	V <sub>CEO(sus)</sub>	600	700	Vdc
Collector-Emitter Voltage	V <sub>CEX</sub>	1300	1500	Vdc
Emitter Base Voltage	V <sub>EB</sub>	5	5	Vdc
Collector Current – Continuous Peak (1)	I <sub>C</sub>	5	7.5	Adc
Base Current – Peak (1)	I <sub>BM</sub>	4	4	Adc
Total Power Dissipation @ T <sub>C</sub> = 95°C Derate above 95°C	P <sub>D</sub>	12.5	0.625	Watts W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +115		°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	1.6	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T <sub>L</sub>	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.



T-33-07

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS (1)</b>					
Collector-Emitter Sustaining Voltage ( $I_C = 100$ mA, $I_B = 0$ )	$V_{CE(sus)}$	600 700	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = 1300$ Vdc, $V_{BE} = 0$ ) ( $V_{CE} = 1500$ Vdc, $V_{BE} = 0$ )	$I_{CES}$	—	—	1.0 1.0	mA
Emitter Base Voltage ( $I_E = 10$ mA, $I_C = 0$ )	$V_{EBO}$	5.0	—	—	Vdc
<b>ON CHARACTERISTICS (1)</b>					
DC Current Gain ( $I_C = 4.5$ Adc, $V_{CE} = 5$ Vdc)	$h_{FE}$	2.25	—	—	—
Collector-Emitter Saturation Voltage ( $I_C = 4.5$ Adc, $I_B = 2$ Adc)	$V_{CE(sat)}$	—	—	5	Vdc
Base-Emitter Saturation Voltage ( $I_C = 4.5$ Adc, $I_B = 2$ Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
<b>DYNAMIC CHARACTERISTICS</b>					
Current-Gain — Bandwidth Product ( $I_C = 0.1$ Adc, $V_{CE} = 5.0$ Vdc, $f_{test} = 1$ MHz)	$f_T$	—	4.0	—	MHz
Output Capacitance ( $V_{CB} = 10$ Vdc, $I_E = 0$ , $f = 0.1$ MHz)	$C_{ob}$	—	125	—	pF
<b>SWITCHING CHARACTERISTICS</b>					
Fall Time ( $I_C = 4.5$ Adc, $I_B = 1.8$ Adc, $L_B = 10$ $\mu$ H, see Figure 1)	$t_f$	—	0.6	—	$\mu$ s

(1) Pulse Test: Pulse Width = 300  $\mu$ s, Duty Cycle < 2%.

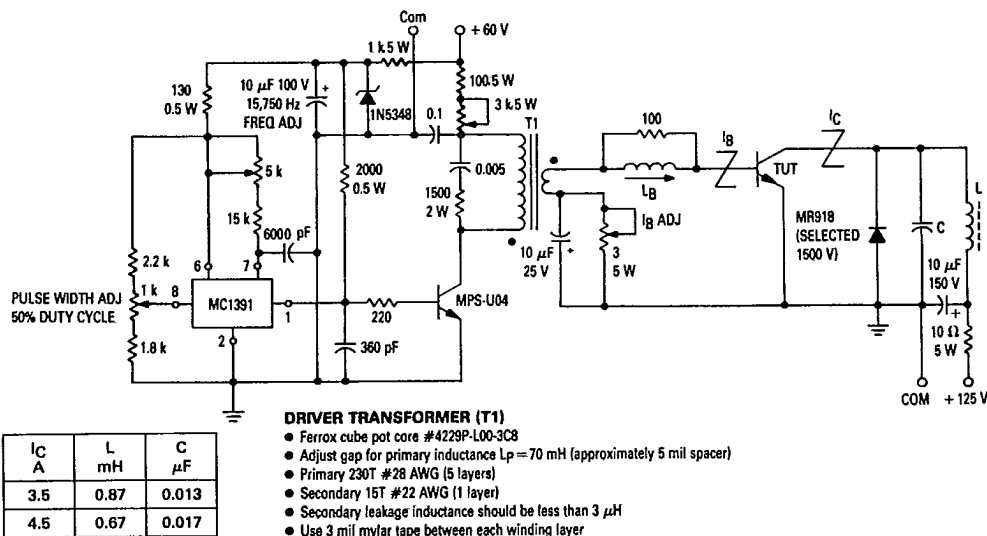


Figure 1. Switching Times Test Circuit

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**BASE DRIVE: The Key to Performance**

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough  $I_{B1}$  to satisfy the lowest gain output device  $h_{FE}$  at the end of scan  $I_{CM}$ . Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right  $L_B$  is usually done empirically, since the equivalent circuit is complex, and since there are several important variables ( $I_{CM}$ ,  $I_{B1}$ , and  $h_{FE}$  at  $I_{CM}$ ). One method is to plot fall time as a function of  $L_B$ , at the desired conditions, for several devices within the  $h_{FE}$  specification. A more informative method is to plot power dissipation versus  $I_{B1}$  for a range of values of  $L_B$  as shown

in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low  $I_{B1}$ ) is caused by saturation losses. The positive slope portion at higher  $I_{B1}$ , and low values of  $L_B$  is due to switching losses as described above. Note that for very low  $L_B$  a very narrow optimum is obtained. This occurs when  $I_{B1} h_{FE} = I_{CM}$ , and therefore would be acceptable only for the "typical" device with constant  $I_{CM}$ . As  $L_B$  is increased, the curves become broader and flatter above the  $I_{B1} h_{FE} = I_{CM}$  point as the turn-off "tails" are brought under control. Eventually, if  $L_B$  is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different  $h_{FE}$ , essentially moves the curves to the left or right according to the relation  $I_{B1} h_{FE} = \text{constant}$ . It then becomes obvious that, for a specified  $I_{CM}$ , an  $L_B$  can be chosen which will give low dissipation over a range of  $h_{FE}$  and/or  $I_{B1}$ . The only remaining decision is to pick  $I_{B1}$  high enough to accommodate the lowest  $h_{FE}$  part specified. Figure 8 gives values recommended for  $L_B$  and  $I_{B1}$  for this device over a wide range of  $I_{CM}$ . These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither  $L_B$  nor  $I_{B1}$  are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

**TEST CIRCUIT WAVEFORMS**

FIGURE 2

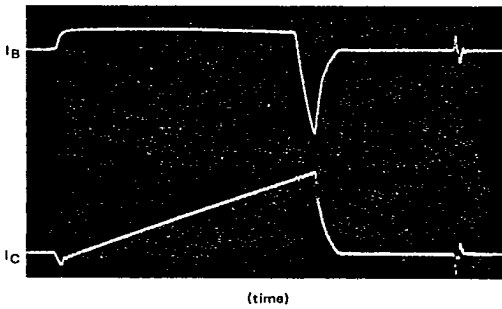
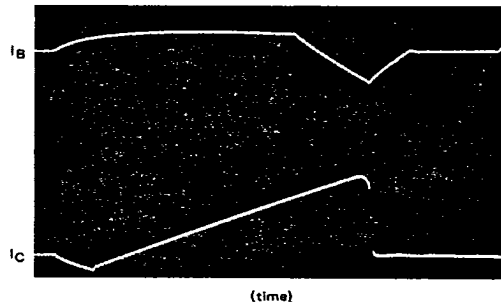


FIGURE 3



3

**TEST CIRCUIT OPTIMIZATION**

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

BU207, BU208

FIGURE 4 - OPTIMIZING DRIVE @  $I_C = 3.5$  A

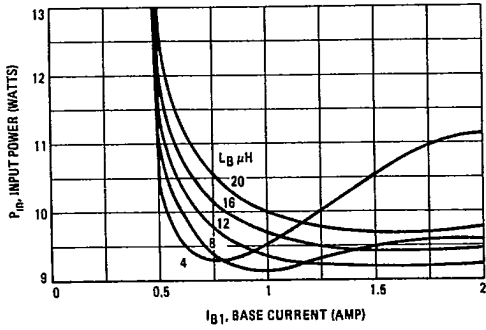


FIGURE 5 - OPTIMIZING DRIVE @  $I_C = 4.5$  A

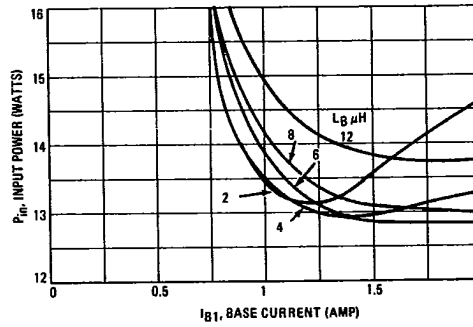


FIGURE 6 - SWITCHING BEHAVIOR versus TEMPERATURE  
 $I_{CM} = 3.5$  A,  $I_B = 1.5$  A,  $L_B = 14 \mu H$

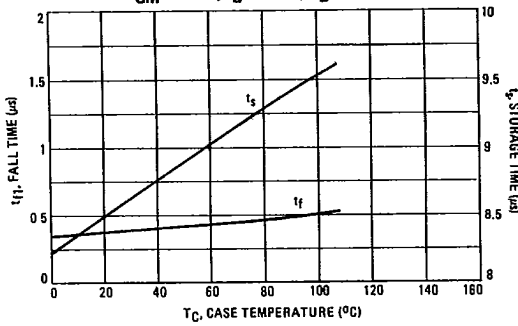


FIGURE 7 - SWITCHING BEHAVIOR versus TEMPERATURE  
 $I_{CM} = 4.5$  A,  $I_B = 1.75$  A,  $L_B = 8 \mu H$

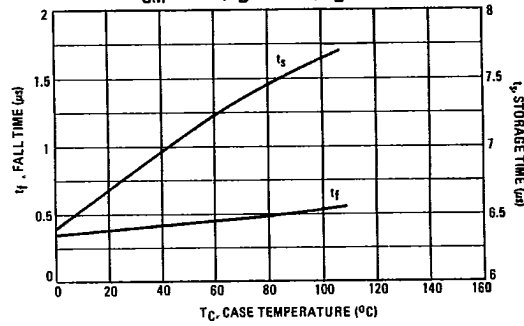


FIGURE 8 - OPTIMUM DRIVE CONDITIONS

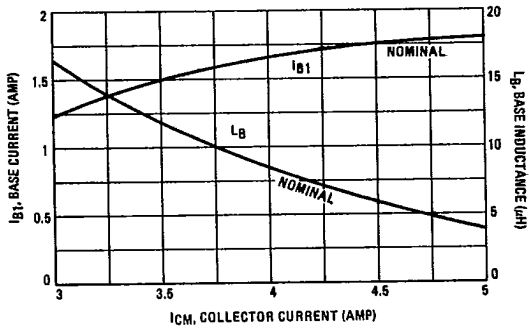
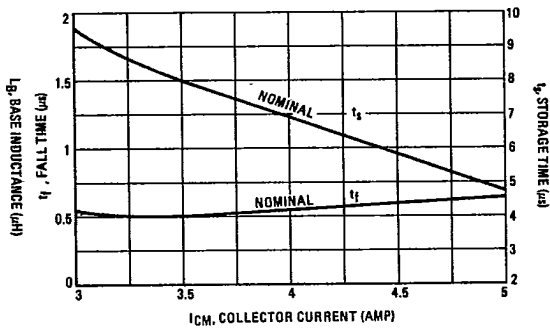


FIGURE 9 - SWITCHING BEHAVIOR versus  $I_{CM}$



T-33-07

FIGURE 10 - THERMAL RESPONSE

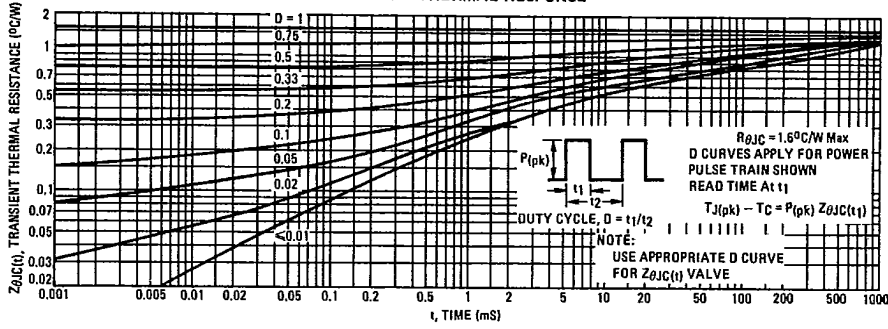


FIGURE 11 - COLLECTOR SATURATION REGION

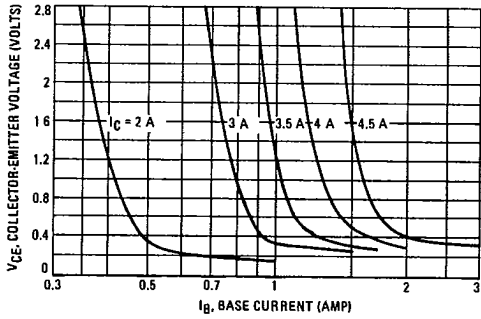


FIGURE 12 - DC CURRENT GAIN

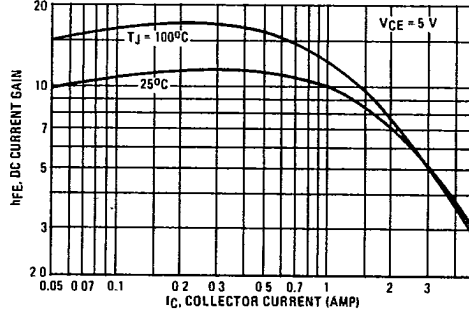


FIGURE 13 - "ON" VOLTAGES

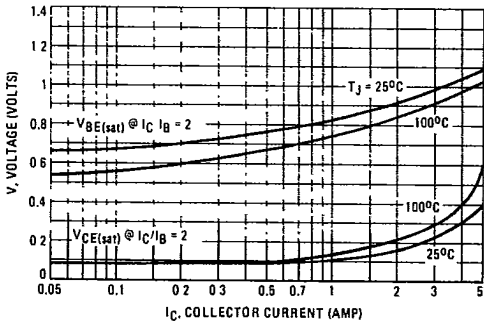
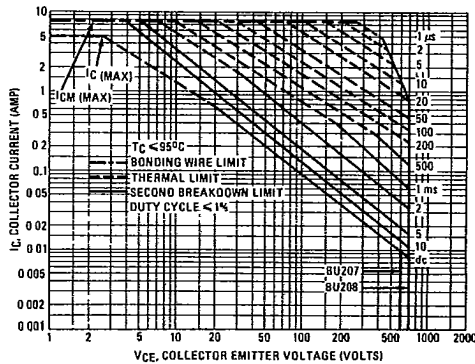


FIGURE 14 - MAXIMUM FORWARD BIAS SAFE OPERATING AREA



3